FoSyn Oscillator

A formant oscillator inspired by Werner Kaegi's VOSIM model with a Flip Flop as the heart of the patch. In this case a so-called RS Flip Flop.

Flip Flop, how it works
R and S stand for successive Reset and Set. If we make the Set input logically one (NMG2 value > 0), the Q output will also be 'high'. The other output with the dash above the Q is the inverting output. This is always opposite to the value of the Q output. We only have to make the S-input high and the output Q remains logically '1'. If we then make the Reset input 'high', then the Q output changes to logic '0' (that is equal to NMG2 value ≤ 0).

Open `RS-FF.pch2`. You see that the Clock input is not used in this application. Experiment with the switches making the Set and Reset inputs logically '1' and '0'. on The output LEDs show how both outputs change from '1' to '0'.

Start-Stop Oscillator
Imagine connecting a delay module to the Q output of the RS Flip Flop and connecting its output to the Reset input while the set input is held logic '1' Then the Reset input will be activated after the set delay time. The Q output is currently reset to '0'. But because the Set input is still logically '1', the process repeats itself.

We now have built an oscillator. The oscillator can be switched on and off with the on-off switch of the Set input. Load `Start-StopOsc.pch2` and tweak the settings and see how it works. If you can simply switch this start-stop oscillator on and off with a switch that alternately sets a logic '1' and '0' on the Set input, then this must also be possible with, for example, a square-wave oscillator: it also produces changes of '1' and '0' at the output.

Load `FormantOsc.pch2` and you will find out how this works. The red oscillator, OscShpA now replaces the on and off switch. This happens very quickly, however, in the pitch domain. You don't now hear the alternately on and off switching but a pitch that corresponds to the set frequency of this fundamental oscillator.

However, switching on and off does not go directly through the output of OscShpA to the Set input of the flip-flop. Instead this is done via a different delay module named pulse. It is a simple delay for only logical signals. The set pulse duration now determines how long the start stop oscillator is on. After the pulse duration has elapsed, the signal at the output becomes '0'. Because this output is connected to the Reset input, the oscillator is stopped. As soon as the fundamental oscillator becomes 'high' again, the Set input will be made '1' again via the pulse delay and our self-built oscillator will start again.

Pulse delay, Envelope & Low Pass Filter
The pulse duration forms a window which determines how many oscillation periods of the start-stop oscillator are present in one period of the fundamental oscillator, or in other words, it concerns the length of the pulse train.

This series of pulses then go into an EnvADR module with which the pulses of the start-stop oscillation subsequently decrease in amplitude. How fast that happens is set with the Decay Rate. Finally, the high frequencies can be attenuated with a low pass filter.

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internet
Rob Hordijks G2 site: everything about
NMG24all.nl/~rhordijk/G2Pages/index.htm